

#6/2-2/02  
Dade

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Divakaruni, et al

Serial No.: 09/718,850

Filed: November 22, 2000



Group Art Unit: 2811

Examiner: G. Munson

For: LOGIC SOI STRUCTURE, PROCESS AND  
APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

Assistant Commissioner of Patents  
Washington, D.C. 20231

RECEIVED  
FEB 13 2002  
TECHNOLOGY CENTER 23000

**SUBMISSION OF FORMAL DRAWINGS**

Sir:

Submitted herewith are twelve (12) sheets of formal drawings comprising Figs. 1-20B for the above-referenced patent application. Acknowledgment of receipt is respectfully requested. Please substitute these formal drawings for the drawings which were filed with the application.

Respectfully Submitted,

Frederick W. Gibb, III

Reg. No. 37,629

Date: 2/15/02  
McGinn & Gibb, PLLC  
2568-A Riva Road  
Suite 304  
Annapolis, MD 21401  
Customer No. 28211

**CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8)**Applicant(s): Divakaruni et al.

Docket No.

**BUR920000016US1**

Serial No.

09/718,850

Filing Date

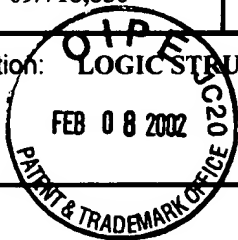
November 22, 2000

Examiner

G. Munson

Group Art Unit

2811

Invention: **LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR**I hereby certify that this **SUBMISSION OF FORMAL DRAWINGS w/Figs. 1-20B**

(Identify type of correspondence)

is being deposited with the United States Postal Service as first class mail in an envelope addressed to: The

Assistant Commissioner for Patents, Washington, D.C. 20231 on

January 15, 2002  
(Date)**Frederick W. Gibb, III**

(Typed or Printed Name of Person Mailing Correspondence)

(Signature of Person Mailing Correspondence)

Note: Each paper must have its own certificate of mailing.

RECEIVED  
FEB 13 2002  
TECHNOLOGY CENTER 2800